

## 2.5A Li-ion Battery Switching Charger with 1A OTG Boost Integrated

### Features

- ◆ Full Automatic and Efficient Charge Management for Large Capacity Lithium Battery
  - Automatic Conditioning, CC/CV Charge Control, Termination and Recharge
  - 20V Input Voltage Tolerance,
  - 5.9V Max Operating Voltage
  - 550-2500mA Programmable Charge Current
  - 1.5MHz Synchronous PWM, 1μH Low Profile Inductor
  - Input Current Regulation Accuracy:  $\pm 5\%$  (100mA and 500mA)
  - Charge Voltage Regulation Accuracy:  $\pm 1\%$
  - Input Voltage Based Dynamic Power Management (VIN DPM)
  - Power Up without Battery
- ◆ Automatic Adaptor Fault Detection
- ◆ High Impedance Mode with Low Power Consumption
- ◆ Comprehensive Protection
  - Reverse Battery Leakage Protection
  - Thermal Regulation and Shutdown
  - Input & Output Over-voltage Protection
- ◆ Built-in Input Current and Input Voltage Limit
- ◆ Integrated Power MOSFET with Max 2.5A Charge Current
- ◆ Automatic Charge and USB Compliant Start Sequence
- ◆ Full Range Programmable Charge Parameter through I<sup>2</sup>C Compatible Interface
- Input Current Limit Threshold
- Input Voltage DPM Threshold
- Charge Termination Current
- Charge Termination Voltage
- Safety Timer with Reset Control (32s/30mins)
- Charge Termination Enable
- Support 3.4MHz I<sup>2</sup>C HS Mode
- ◆ USB OTG Boost
  - Input Voltage Range from Battery: 2.5V~4.5V
  - 5.0V/1000mA ( $V_{BAT} \geq 3.0V$ )
- ◆ 20-Pin WLCSP Package
- ◆ Pin Compatible with HL7005

### Applications

- Smart phone
- MP3 player
- Tablet PC

<b>Part Number</b>	<b>HL7007</b>
Default Charge Termination Voltage	4.2V
Maximum Charge Current	2.5A
OTG Mode Maximum Output Current	1A
I <sup>2</sup> C Address	6AH
30min Safety Timer and 32s Watch-Dog Timer	Yes
Package	WLCSP
Packing Method	Tape and Reel

Figure 1. HL700 Typical Application Diagram

Component	Part Number	Value	Size	Vendor
L1	LQM2MPN1R0	1μH	2016	Murata
Cicsp, Cicsn	C1005X5R1A104K	0.1μF	0402	TDK
Cboot	C2012X5R1E003K	33nF	0805	TDK
Cusb	C2012X5R1E105K	1μF	0805	TDK
Cprt	C2012X5R1E475K	4.7μF	0805	TDK
Cref	C1005X5R1A105K	1μF	0402	TDK
Cout1,Cout2	GRM319R61A226ME15D	22μF	1206	Murata
Rsns	-	33mΩ	1206	-
R1,R2	-	1kΩ	-	-
R3,R4,R5	-	10kΩ	-	-

Table 1 Recommended Component list

## Description

HL7007 is a compact, flexible, high-efficiency, USB compliant switch-mode charge management device for single cell Li-ion and Li-polymer battery used in a wide range of portable applications. The charge parameters can be programmed through I<sup>2</sup>C interface. HL7007 integrates a synchronous PWM controller, power MOSFET, input current sensing, high-accuracy current and voltage regulation, and charge termination function into a tiny CSP package.

HL7007 provides a complete automatic three-phase battery charging control: trickle charge, constant-current charge (CC) and constant voltage charge (CV) until the battery reaches the charge termination voltage. The input current is automatically limited to the value set by the host. Charging is terminated based on the battery voltage and a

user selectable minimum current level. A safety timer with reset control provides a safety backup for I<sup>2</sup>C interface. During normal operation, the IC automatically restarts the charge cycle if the battery voltage falls below an internal threshold and automatically enters sleep mode or high impedance mode when the input supply is not correctly connected. The charge status can be reported to the host through the I<sup>2</sup>C interface.

During the charging process, the IC monitors its junction temperature (T<sub>J</sub>) and reduces the charge current once T<sub>J</sub> increases to about 120°C. To support USB OTG device, HL7007 can provide VBUS (5.0V) by boosting the battery voltage.

HL7007 is available in a 20 pin WLCSP package.

## Pin Function

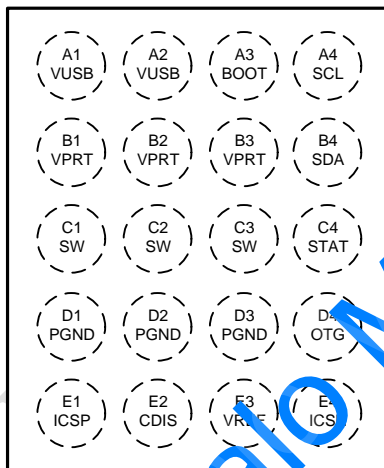


Figure 2. (Top View)

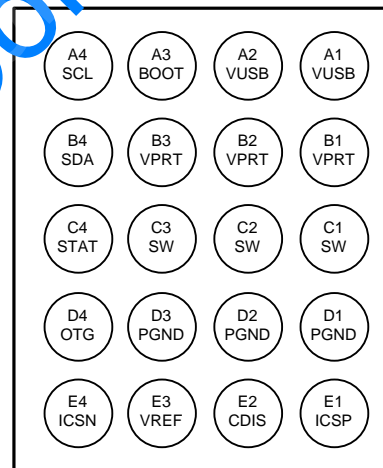


Figure 3. (Bottom View)

## Pin Description

PIN No.	PIN Name	I/O	Description
E4	ICSN	I	Battery voltage and current detection input. If there is a long trace connected to the battery, a ceramic capacitor ( min 0.1 $\mu$ F) connected to PGND is required.
A1, A2	VUSB	I/O	Charger input voltage. Connecting a 1 $\mu$ F capacitor from VUSB to PGND. In the boost mode, it provides power to the load.
B1, B2, B3	VPRT	I/O	Connection point between reverse blocking FET and high side FET. Place a 4.7 $\mu$ F ceramic capacitor from VPRT to PGND.
C1, C2, C3	SW	O	Switch mode buck regulator output.
A3	BOOT	I/O	Connection point of bootstrap capacitor driven by High side FET. Place a 10-33nF ceramic capacitor from BOOT to SW.
D1, D2, D3	PGND		Power ground.
E1	ICSP	I	Charge current sense input. Connect to the precision sense resistor in series with the battery. Bypass this pin with a 0.1 $\mu$ F ceramic capacitor to PGND.
A4	SCL	I	I <sup>2</sup> C interface serial clock. Connect SCL to 1.8V rail through a 1-10k $\Omega$ pull-up resistor.
B4	SDA	I/O	I <sup>2</sup> C interface serial data. Connect SDA to 1.8V rail through a 1-10k $\Omega$ pull-up resistor.
C4	STAT	O	Charge status pin, open-drain. =Low when charge in progress, =HZ for other conditions. During faults, a pulse with 128- $\mu$ s cycle is sent out. STAT pin can be disabled by the EN_STAT bit in control register. STAT can be used to drive an LED indicator or communicate with a host processor.
E3	VREF	O	Internal regulator bypass output. Connect a 4.7 $\mu$ F ceramic capacitor from this output to PGND. External load on VREF is not recommended.
E2	CDIS	I	CDIS charge disable control pin. =0: charge is enabled; =1: charge is disabled and high impedance mode from VUSB to GND
D4	OTG	I	Boost mode enable control or selection pin for input current limit. 1. When OTG mode is in active, OTG enables IC to operate in boost mode. It has higher priority over I <sup>2</sup> C control and can be disabled using the control register. 2. After POR without a host, OTG is used to select input current limit. The input current and threshold set by I <sup>2</sup> C register is not used.

When OTG=1, IINLIM=500mA; when OTG=0, IINLIM=500mA.

Table 2 HL7007 Pin Description

## Internal Functional Block Diagram

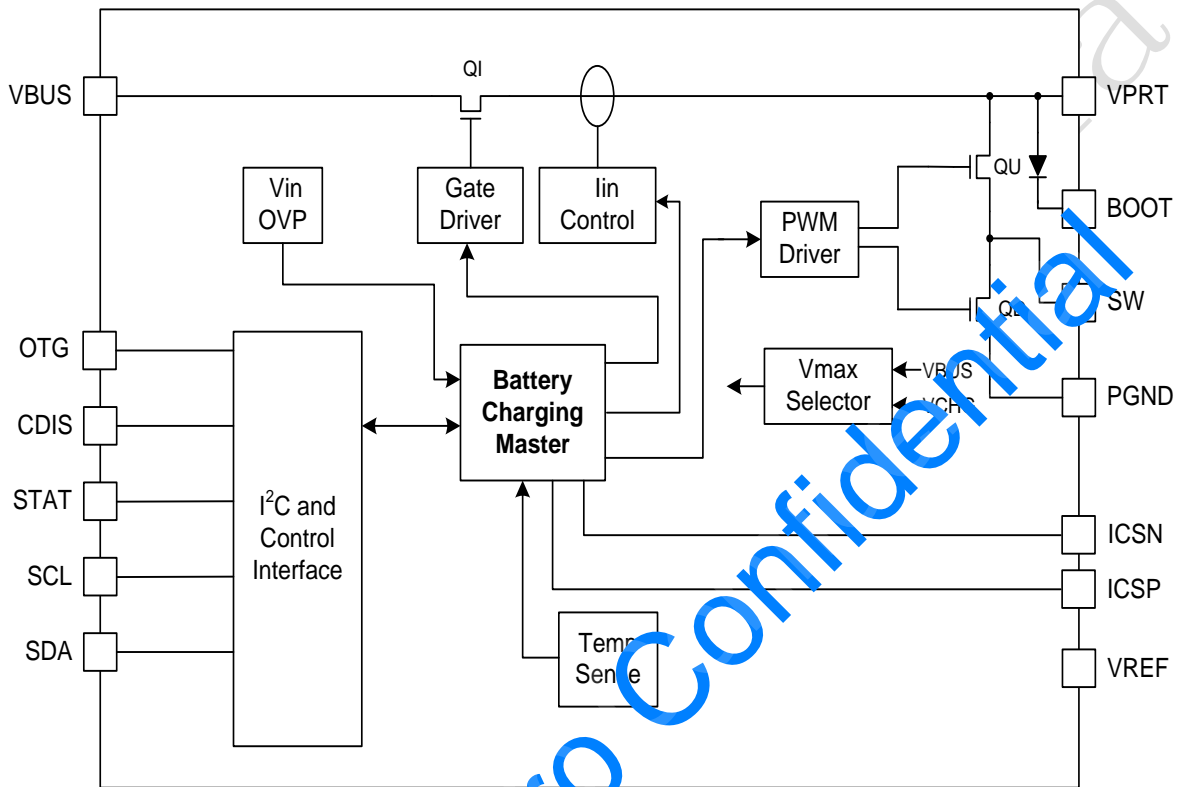


Figure 4. HL7007 Internal Functional Block Diagram

## Absolute Maximum Ratings<sup>(1)</sup>

$V_{USB}$ pin voltage	-1V ~ 20V
$V_{PRT}$ , BOOT pin voltage	-0.3V ~ 20V
SW pin voltage : IC Not Switching	-0.3V ~ 7V
IC Switching	-0.3V ~ 5.9V
Other pin voltage	-0.3V ~ 5.5V
IC power, $P_D@25^\circ\text{C}$	1.17W
Junction-to-ambient thermal resistance, $\theta_{JA}$	85°C/W
Junction-to-case thermal resistance, $\theta_{JC}$	25°C/W
Junction temperature, $T_J$	-40°C ~ 125°C
Storage temperature, $T_{stg}$	-65°C ~ 150°C
Pin soldering temperature, $T_s(10s)$	260°C
ESD: HBM	2kV
ESD: CDM	2kV

## Recommended Operating Conditions<sup>(2)</sup>

$V_{USB}$ , $V_{PRT}$ , SW pin Voltage	4.3V ~ 5.5V
Operating free-air temperature, $T_A$	-30°C ~ 85°C
Junction temperature, $T_J$	-30°C ~ 120°C

### Note

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +85°C unless otherwise noted.

## Electrical Specifications

### Electrical specifications of Charge and OTG boost function

$V_{USB} = 5V$ ,  $HZ\_MODE = 0$ ,  $OPA\_MODE = 0$  ( $CDIS = 0$ ),  $T_A = -40^{\circ}C$  to  $125^{\circ}C$ . And  $T_A = 25^{\circ}C$  unless Otherwise Noted.

Parameter		Test Condition	Min	Type	Max	Unit
Input Current						
I <sub>USB</sub>	V <sub>USB</sub> current control	V <sub>USB</sub> > V <sub>USB (min)</sub> , PWM work		10		mA
		V <sub>USB</sub> > V <sub>USB (min)</sub> , PWM Stop			5	
		0°C < T <sub>A</sub> < 85°C , CD=1 or HZ_MODE=1		850		μA
I <sub>lgk</sub>	Battery leakage to V <sub>USB</sub>	0°C< T <sub>A</sub> < 85°C,V <sub>ICSN</sub> =4.2V In High-Z mode, V <sub>USB</sub> =0V, Test V <sub>USB</sub> current			5	μA
	In High-Z mode, battery discharge current(input from Pin ICSN,ICSP&SW to IC)	0°C < T <sub>A</sub> < 85°C,V <sub>ICSN</sub> =4.2 V, In High-Z MODE,V = 0V , SCL,SDA,OTG = 0V or 1.8 V			22	μA
Charge Termination Voltage						
V <sub>OREG</sub>	Output cutoff voltage setting range	Work in cutoff voltage, programmable	3.5		4.44	V
	Cut off Voltage precision	T <sub>A</sub> = 25°C	−1		1	%
		T <sub>J</sub> =0-125°C	−2		2	%
Charge Current (Fast Charge)						
I <sub>oCHARGE</sub>	Output charge current setting range	V <sub>SHORT</sub> ≤ V <sub>ICSN</sub> < V <sub>OREG</sub> , R <sub>SNS</sub> =68mΩ, IO_LEVEL=0,programmable	550		2450	mA
	Low charge current (enable default value after 30mins mode)	V <sub>SHORT</sub> ≤ V <sub>ICSN</sub> < V <sub>OREG</sub> , R <sub>SNS</sub> =68mΩ,IO_LEVEL=1, OTG=High	475	500	525	mA
	Cut off voltage precision calculated through R <sub>(SNS)</sub> (base on charge current) V <sub>IREG</sub> =I <sub>oCHARGE</sub> × R <sub>SNS</sub>		−5		5	%
Weak Battery Detection						
V <sub>LOWV</sub>	Weak battery voltage limit threshold programmable scale <sup>Note 1</sup>	Programmable through I <sup>2</sup> C control	3.4		3.7	V
	Weak battery voltage		−5		5	%

	accuracy						
	Anti peak delay of weak battery threshold	Rising voltage, 2mV over drive, $t_{RISE} = 100 \text{ ns}$		32		ms	
CDIS & OTG Pin Logic Level							
$V_{IL}$	Input low threshold level				0.4	V	
$V_{IH}$	Input high threshold level		1.2			V	
$I_{bias}$	Input bias current	Voltage on control pin: 1.8 V			1.0	$\mu\text{A}$	
Charge Termination Detection							
$I_{TERM}$	The termination charging current programmable range	$V_{ICSN} > V_{OREG} - V_{RCH}$ , $R_{SNS}=68 \text{ m}\Omega$ , programmable	50		400	mA	
	Anti peak delay of termination charge	The rise and fall, 2mV overdrive, $t_{RISE}, t_{FALL} = 100 \text{ ns}$		32		ms	
	Through $R_{SNS}$ termination current adjust accuracy $V_{IREG\_TERM} = I_{TERM} \times R_{SNS}$	$3.4 \text{ mV} \leq V_{(IREG\_TERM)} \leq 6.8 \text{ mV}$	-20		20	%	
		$6.8 \text{ mV} < V_{(IREG\_TERM)} \leq 17 \text{ mV}$	-10		10		
		$17\text{mV} < V_{IREG\_TERM} \leq 27.2 \text{ mV}$	-5		5.5		
Adapter Detection							
$V_{USB (min)}$	Input voltage limit <sub>(min)</sub>	Adapter detection	3.8	4	4.2	V	
	Anti peak delay when $V_{USB}$ rise to $V_{USB (min)}$	Rising voltage, 2mV overdrive, $t_{RISE} = 100 \text{ ns}$		32		ms	
	$V_{USB (min)}$ hysteresis	Input voltage rising		200		mV	
$I_{USB\_DETECT}$	From the current source to the GND	During the detection of adapter		50		mA	
$t_{INT}$	Detection time interval	The input power detection		2		S	
Input Based on Dynamic Power Management							
$V_{USB\_DPM}$	The input voltage DPM threshold programmable range		4.213		4.773	V	
	$V_{USB\_DPM}$ threshold accuracy		-2		2	%	
Input Current Limit							
$I_{IN\_LIMIT}$	The input current limit threshold	$I_{IN} = 100\text{mA}$	$T_A = 0^{\circ}\text{C}\sim 125^{\circ}\text{C}$	86	93	100	mA
		$I_{IN} = 500\text{mA}$	$T_A = 0^{\circ}\text{C}\sim 125^{\circ}\text{C}$	450	475	500	mA
VREF Internal Bias Reference Comparator							
$V_{REF}$	Internal bias voltage reference	$V_{USB} > V_{USBN(min)}$ or $V_{VREF} = 1$ , $C_{VREF}=4.7\mu\text{F}$	3.8		5.9	V	
The Battery Recharge Threshold							



$V_{RCH}$	Recharge threshold voltage	Below $V_{OREG}$	100	120	150	mV
	Anti peak delay	$V_{ICSN}$ reduce below threshold, $t_{FALL}=100ns$ , 10mV overdrive		128		ms
<b>The State of Output</b>						
$V_{OL(STAT)}$	Low level output saturation voltage, STAT pin	$I_O = 10\text{ mA}$ , sink current			0.4	V
	STAT High level leakage current	STAT pin voltage :5.5 V			1	$\mu A$
<b>I<sup>2</sup>C Bus Logic Level&amp; Timing</b>						
$V_{OL}$	The output of low threshold level	$I_O = 10\text{ mA}$ , sink current			0.4	V
$V_{IL}$	Input low threshold level	$V_{pull-up} = 1.8\text{ V}$ , SDA & SCL			0.4	V
$V_{IH}$	Input high threshold level	$V_{pull-up} = 1.8\text{ V}$ , SDA & SCL	1.2			V
$I_{BIAS}$	input bias current	$V_{pull-up} = 1.8\text{ V}$ , SDA & SCL			1	$\mu A$
$f_{SCL}$	SCL clock frequency				3.4	MHz
<b>Battery Detection</b>						
$I_{DETECT}$	The battery detection current, before the charging is completed (sink current)	Start after terminated detection, $V_{ICSN} \leq V_{OREG}$		2		mA
$t_{DETECT}$	Battery detection time			256		ms
<b>Sleep Mode Parameters</b>						
$V_{SLP}$	Sleep-mode threshold $V_{USB} - V_{ICSN}$	$1.3\text{ V} \leq V_{ICSN} \leq V_{OREG}$ , $V_{USB}$ clamping		0		mV
$V_{SLP\_EXIT}$	Sleep-mode Exit hysteresis	$1.3\text{ V} \leq V_{ICSN} \leq V_{OREG}$		80		mV
	$V_{USB}$ rise to $V_{SLP} + V_{SLP\_EXIT}$ Anti peak delay	Rising voltage, 2mV overdrive, $t_{RISE} = 100\text{ ns}$		32		ms
<b>PWM</b>						
Voltage between BOOT pin & SW pin		During charging or boosting period			6.5	V
Q1: The input FET conduction resistance		$I_{IN\_LIMIT} = 500\text{ mA}$ , Measure between $V_{USB}$ and $V_{PRT}$		130		m $\Omega$
QU:The high -side FET conduction resistance		Measure between SW and $V_{PRT}$ , $V_{BOOT} - V_{SW} = 4\text{ V}$		100		
QD: The low-side FET conduction resistance		Measure between SW and PGND		96		

f <sub>OSC</sub>	Oscillator frequency			3.0		MHz
	Frequency accuracy		-10		10	%
D <sub>MAX</sub>	Max duty cycle			98		
D <sub>MIN</sub>	Min duty cycle		0			
Charge Mode Protection						
V <sub>OVP_IN_USB</sub>	V <sub>USB</sub> OVP threshold voltage	V <sub>BUS</sub> reach threshold during charge period and turn off converter	5.7	5.8	6.1	V
	V <sub>OVP_IN_USB</sub> hysteresis	V <sub>USB</sub> fall down to V <sub>OVP_IN_USB</sub>		200		mV
I <sub>LIMIT</sub>	During charging, cycle by cycle current limit	Work in charge mode		2.9		A
V <sub>SHORT</sub>	Short circuit charge cycle voltage threshold	V <sub>(ICSN)</sub> rise	1.9	2.0	2.1	V
	V <sub>SHORT</sub> hysteresis	V <sub>(ICSN)</sub> fall below V <sub>SHORT</sub>		100		mV
I <sub>SHORT</sub>	The trickle charge current	V <sub>(ICSN)</sub> ≤ V <sub>SHORT</sub>	20	30	40	mA
Boost Mode (OPA_MODE = 1, HZ_MODE = 0)						
V <sub>USB_B</sub>	Output voltage (to V <sub>USB</sub> pin )	2.5V < V <sub>(ICSN)</sub> < 4.5 V		5.0		V
	Output voltage accuracy	Including the line and load regulation	-3%		3%	
I <sub>BO</sub>	Max output current	3.0 V < V <sub>(ICSN)</sub> < 4.5 V	650			mA
I <sub>BLIMIT</sub>	Cycle current limit	2.5 V < V <sub>(ICSN)</sub> < 4.5 V		1.8		A
V <sub>USBOVP</sub>	Overvoltage protection threshold (V <sub>USB</sub> Pin)	If boosting period threshold exceed V <sub>USB</sub> , shut down converter	5.7	5.9	6.1	V
	V <sub>USBOVP</sub> hysteresis	V <sub>USB</sub> turn down from V <sub>USBOVP</sub>		200		mV
V <sub>BATMIN</sub>	Min battery voltage (ICSN Pin)	In boosting period		2.5		V
		Ahead of Boost start	2.8	2.9	3.0	V
Protection						
T <sub>SHTDWN</sub>	Over temperature protection			145		°C
	Temperature hysteresis			20		
T <sub>CF</sub>	Over temperature current limit	Charges current start to decline		120		

$t_{32S}$	32 seconds Watchdog timer	32 seconds mode or HOST mode	15	32		s
$T_{30M}$	30 minutes safety timer	30 minutes mode	15	30		m

Table 3. Electrical Specifications

## Note:

- (1) In 30 minutes mode of HL7007, if the battery is charged to a higher voltage than the termination voltage, charger will enter Hi-Z mode and wait for the I<sup>2</sup>C command.

## Typical Characteristics

$V_{USB} = 5V$ ,  $V_{BAT} = 3.6V$ ,  $I_{OCHARGE} = 1450mA$ ,  $T_A = 25^\circ C$  unless otherwise noted.

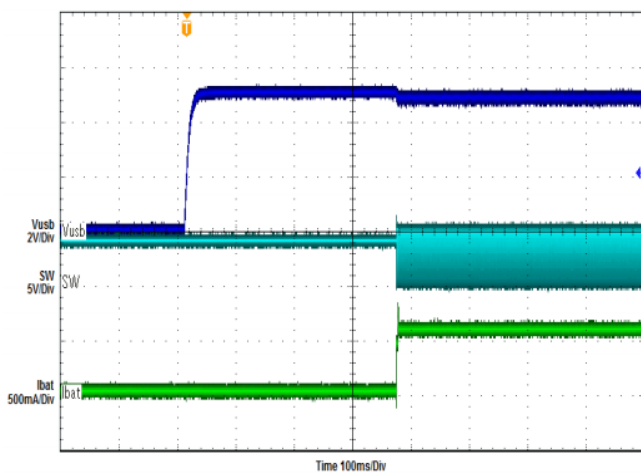


Figure 5. Auto-Charge Startup at VBUS Plug in  
( $I_{OCHARGE} = 550mA$ )

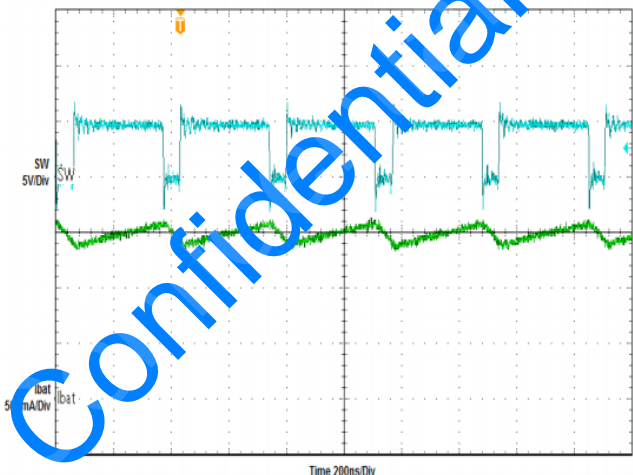


Figure 6. PWM Charging waveform

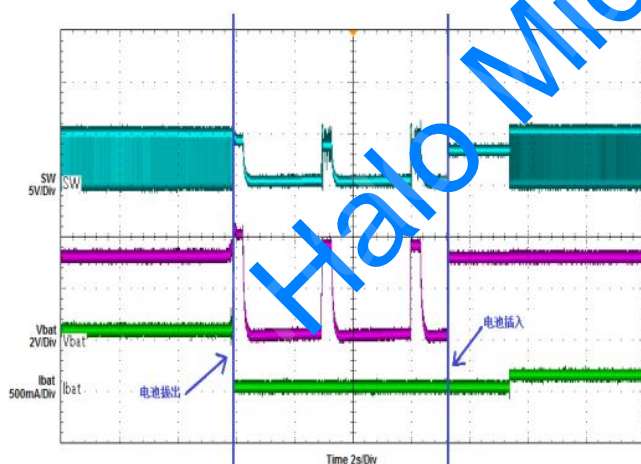


Figure 7. Battery Removal/ Insertion During Charging  
( $V_{BAT} = 3.2V$ ,  $I_{IN\_LIMIT} = 500mA$ )

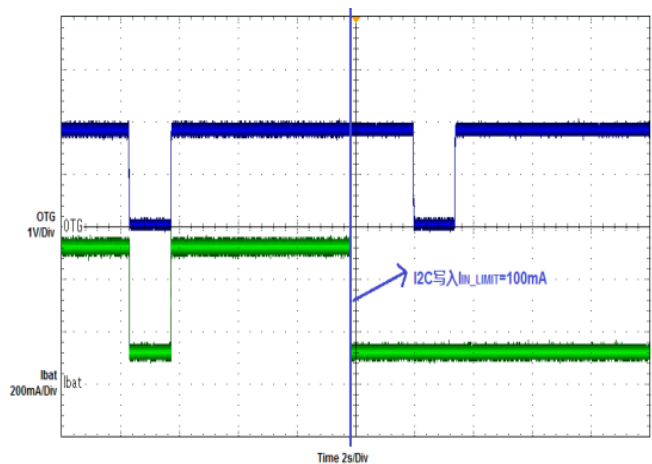


Figure 8. Auto-Charge Startup with Limited Current  
( $V_{BAT} = 3.0V$ ,  $I_{IN\_LIMIT} = 100/500mA$ )

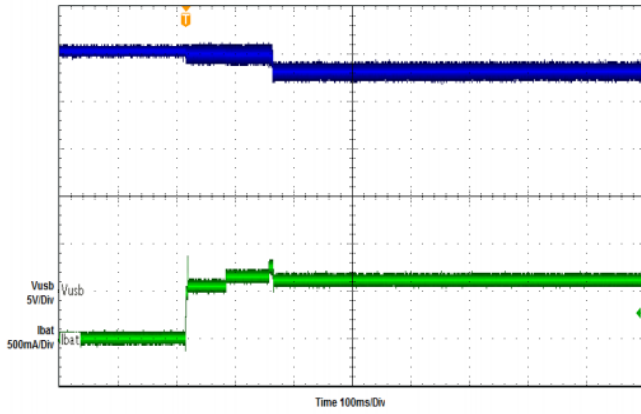


Figure 9. Input Voltage Dynamic Control

(VUSB=5V/500mA LIMIT, VUSB\_DPM=4.533V)

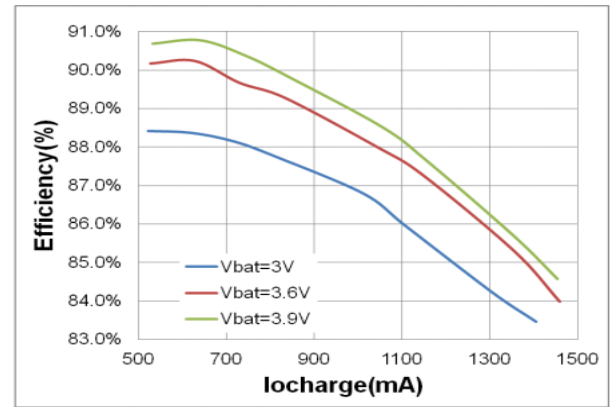


Figure 10. Charger Efficiency

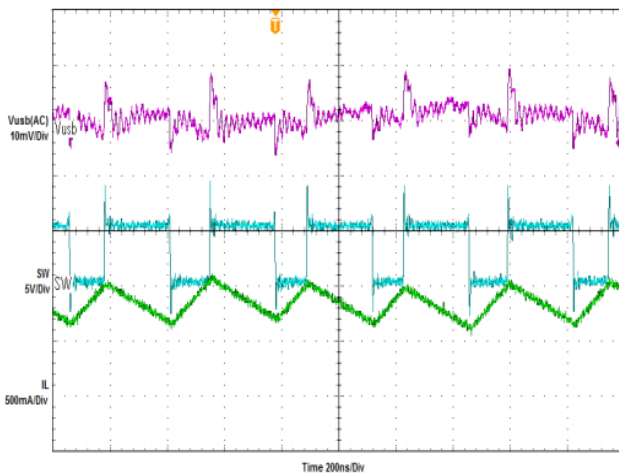


Figure 11. Boost PWM Waveform (IUSB=500mA)

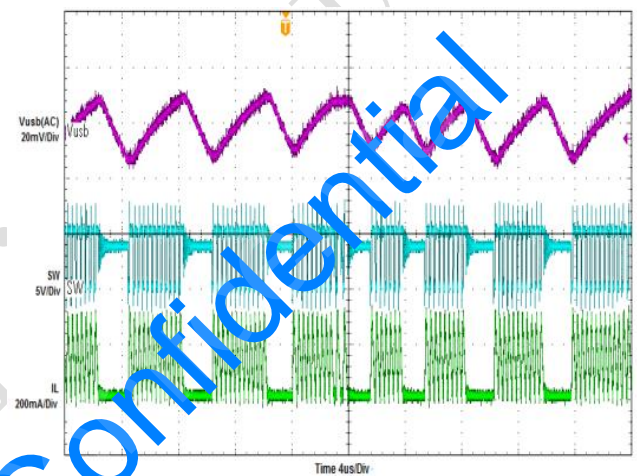


Figure 12. Boost PFM Waveform (IUSB=50mA)

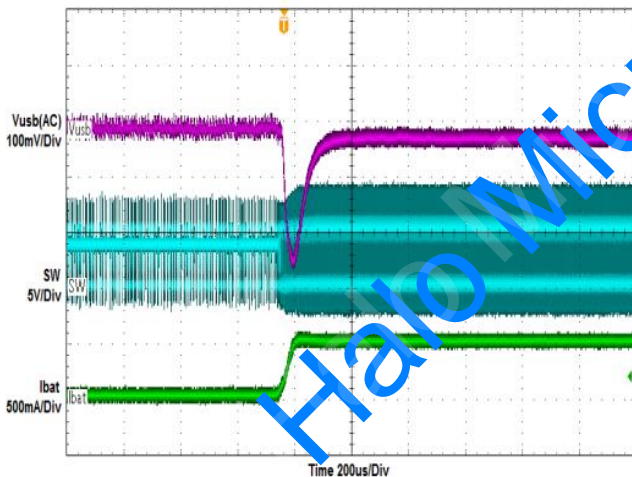


Figure 13. Boost mode load transient (IUSB=0mA->500mA)

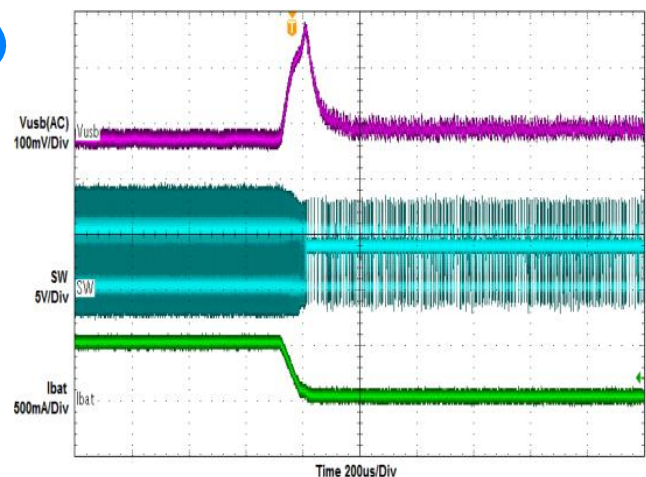


Figure 14. Boost mode load transient (IUSB=500mA->0mA)

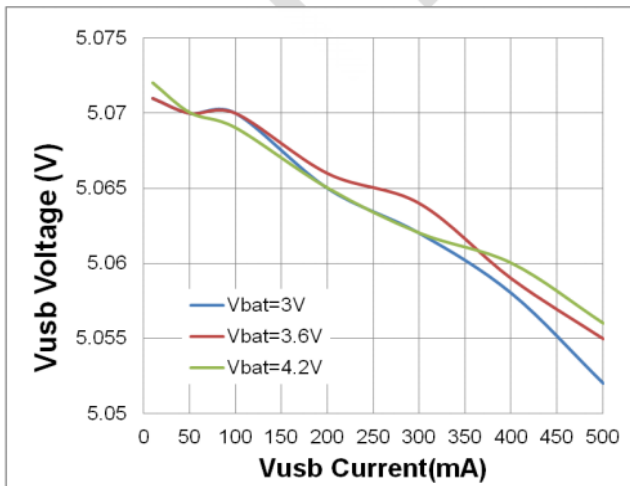


Figure 15. Boost Load Regulation

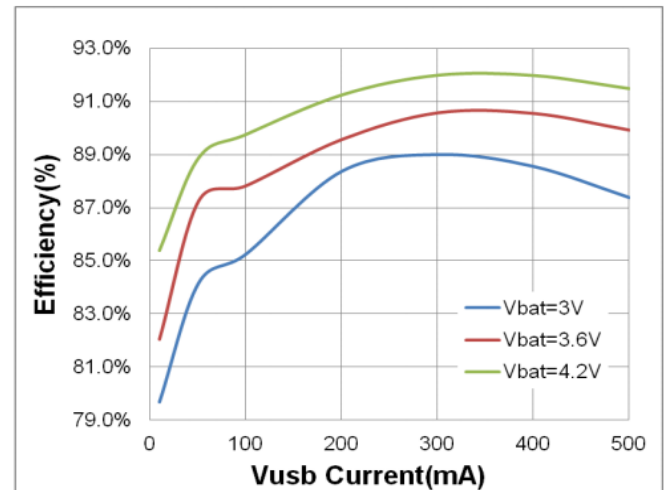


Figure 16. Boost Efficiency

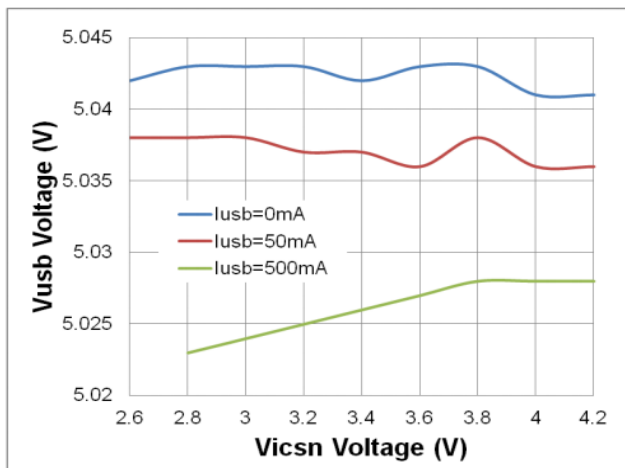


Figure 17. Boost Line regulation

## Detailed Description

HL7007 provides complete automatic three-phase battery charging and management: constant pre-charge, high current switching-mode constant current (CC) charge and constant voltage (CV) charge until the battery voltage rises to the termination voltage. When the battery voltage drops below the internal threshold limit, the IC will automatically restart a charging cycle. If the input power supply is disconnected, the IC will automatically enter the high-Z mode to prevent the battery from being dissipated. When the IC's temperature rises to 120°C, it will automatically reduce the charging current to prevent the IC from overheating.

HL7007 has three operation modes: charge mode, boost mode and high-Z mode. In the charge mode, the IC supports a single lithium-ion battery or lithium-polymer battery to be accurately charged. In the boost mode, the IC will boost the battery voltage and provide power to the OTG device connected to the VUSB pin. In the high-Z mode, the IC stops operation and enters high impedance state. In this state, the current consumption from the VUSB terminal and from the battery terminal is minimized. When the handheld device is in standby state, this mode can effectively reduce the IC power consumption.

The host communicates through I<sup>2</sup>C (HCR mode or 32 seconds mode) to control the IC to operate in different modes. If the I<sup>2</sup>C host is absent, the IC will start the 30-minute safety timer and enter the 30-minute (default) mode, in which the charger will continue charging the battery using default register value and charging parameters until the safety timer times out. After that, the charger stops and enter HZ mode.

## IC Operation in Charge Mode

When a good battery with voltage below recharge threshold limit is inserted, and a good adapter is detected, HL7007 enters the charge mode. In this mode the IC has 5 control loops to regulate the input voltage, input current, charging current, charging voltage and IC temperature.

During the charging period, all 5 loops are enabled and one of them is in control. Figure 18(a) shows a typical charging curve without inputting current regulation loop. This is a standard Li-Ion battery CC/CV charging curve. Figure 18 (b) shows in the CC mode, a typical charging curve with the IC's input current is limited.

In a switched-mode charger like HL7007, the charge current is higher than the input current; therefore the charging process will be faster than the traditional linear charge scheme. In HL7007, input voltage limit threshold of the dynamic power management (DPM) loop, input current, charge current, termination current and termination voltage etc. can all be set by the I<sup>2</sup>C interface.

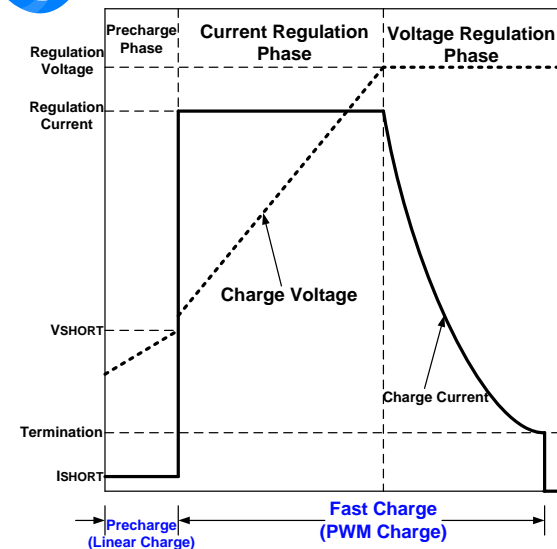


Figure 18(a) Typical charging curve without input current limit



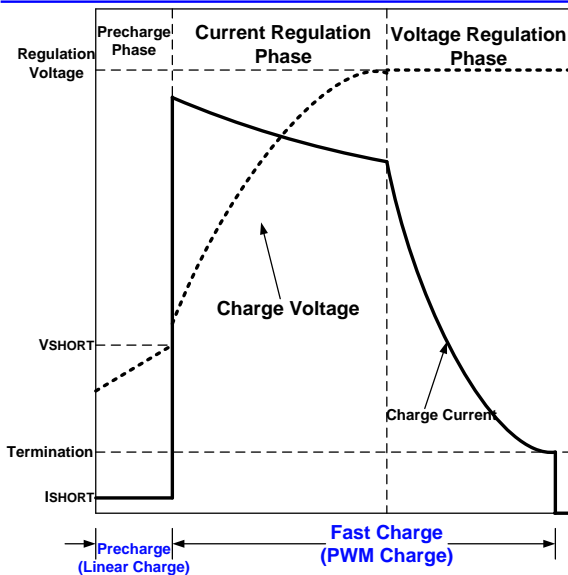


Figure 18(b) Charging curve with input current limit

## PWM Controller in Charge Mode

HL7007 provides a highly efficient synchronous 3MHz PWM controller to regulate the charging current and voltage. Power MOSFETS are also integrated. Its duty cycle ranges from 0% to 95%.

HL7007 has three NMOS power MOSFET: input reverse-blocking FET Q1, high-side FET QU and low-side FET QD. When  $V_{USB}$  is lower than  $V_{ICSN}$ , Q1 prevents battery from discharging to  $V_{USB}$ . A charge pump circuit is used to provide gate drive for Q1, while a bootstrap circuit with an external bootstrap capacitor is used to supply the gate drive of Q2.

Cycle-by-cycle (CBC) current limit is implemented in QU for safe operation and output short-circuit protection.

## Battery Charge Process

When the battery voltage is lower than  $V_{(SHORT)}$  threshold, the IC provides a trickle current  $I_{(SHORT)}$  to the battery. When the battery voltage rises to between  $V_{SHORT}$  and  $V_{OREG}$ , The charger enters CC phase by increasing charge current to quick charge current  $I_{OCHARGE}$ , or a value matching the input current limit  $I_{IN\_LIM}$  if that threshold is reached.

Built-in soft-start scheme slowly increases the quick charge current to its target value to minimize current and voltage overshoot on the battery. Both the input current limit  $I_{IN\_LIMIT}$  and quick charge current  $I_{OCHARGE}$  can be set by the host. Once the battery voltage reaches the regulation voltage  $V_{OREG}$ , the charger enters CV phase, and the charge current tapers down as shown in Figure 4. Regulation of the voltage loop is based on monitoring the voltage between ICSN and PGND and compare against an internal reference voltage. In HOST mode, the regulation voltage is set between 3.5V to 4.44V. In 30-minute mode, the regulation voltage is fixed at 4.2V.

During the CV phase, HL7007 also monitors the charge current. In HOST mode with charge termination enabled ( $TE=1$ ), the IC will turn off charging if ICSN pin voltage is higher than the battery recharge threshold  $V_{OREG}-V_{RCH}$  for more than 32 ms (typical), and measured charge current is less than the termination charge current  $I_{TERM}$ . At this time, IC will turn on a discharge current  $I_{DETECT}$  on ICSN pin for  $t_{DETECT}$  (typical 256ms), then check the battery voltage. If the battery voltage is still higher than the recharge threshold after  $t_{DETECT}$ , the battery charging is complete. The battery detection routine is used to ensure charge termination does not occur because the battery is removed. The STAT bits and STAT pin are updated to indicate charge completion. The host can program charge termination current level, as well as disabling charge termination function by setting termination bit (TE) to 0.

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the  $V_{OREG} - V_{RCH}$  threshold.
- VBUS Power-on reset (POR), if battery voltage is below the  $V_{(LOWV)}$  threshold.
- Bit of  $\overline{CE}$  toggles or RESET bit is set (under Host

control)

## Operation in Boost mode

In 32-second mode, the host can enable HL7007's boost mode operation through one of the following two methods:

1. Set OTG\_EN=1, OTG\_PL=1(default), then set OTG pin=1. Or set OTG\_EN=1, OTG\_PL=0, then set OTG pin=0;
2. Set OPA\_Mode =1

In boost mode, the IC provides 5V output to the USB port. The maximum output current no less than 650mA ( $I_{BO}$ ) when battery voltage is 3.0V or higher.

## PWM Controller in Boost Mode

Similar to the charge mode, HL7007 provides an integrated PWM controller in boost mode to regulate VUSB pin voltage. CBC current limit of 1.6A on the low-side power MOSFET QD provides output overload and short-circuit protection.

## Boost Start-Up and Protection

HL7007 has built-in boost soft start sequence to prevent battery in-rush current and inductor current saturation. The IC also provides battery under-voltage, output over-voltage and chip over-temperature protection.

## Boost PFM Mode

Under light load conditions, the IC operates in PFM mode to reduce the power loss and maintain converter efficiency. During boosting, the PWM converter is turned off once the inductor current is less than 0mA, and the PWM will start switching only when VSUB voltage drops below output target voltage. HL7007 automatically switches between PWM and PFM mode depending on load conditions.

## Safety Timer in Boost Mode

At the beginning of boost operation, the IC starts a 32-second timer. It is reset by the host using the I<sup>2</sup>C interface.

Writing "1" to reset bit of TMR\_RST in control register will reset the 32-second timer and TMR\_RST is automatically set to "0" after the 32 second timer is reset. Once the 32-second timer expires, the IC exits the boost mode, enables the fault pulse on the STAT pin and sets fault status bit in the status register. The fault condition is cleared by POR or host control.

## HIGH IMPEDANCE (Hi-Z) MODE

In Hi-Z mode, the charger stops charging and enters a low quiescent current state to conserve power. The chip enters High-Z mode if one of the following conditions are met.

1. Set CDIS pin =1.
2. In 30-minute mode and CDIS pin=0:  $V_{BUS} > V_{BUS(min)}$  and battery present with  $V_{BAT} > V_{LOWV}$ .
3. In host mode, CDIS pin=0, OTG\_EN=0: set HZ\_MODE bit =1.

If HL7007 enters High-Z state in 30-minute mode, CDIS pin=0, and the battery voltage  $V_{BAT} < V_{(LOWV)}$ , the 32-second timer is activated to wait for the host control. Once the 32-second timer expires, the IC re-enters 30 minute mode and 32-second timer is disabled.

If HL7007 enters HiZ state in host mode, CDIS pin=0, and  $V_{BUS} > V_{BUS(min)}$ , IC can exit Hi-Z mode by writing "0" to the HZ-MODE control bit.

In the 30-minute mode, set CDIS pin=1 resets the 30-minute timer.

## Other Functions

HL7007 has comprehensive fault reports. Please refer to the Application Information section for detailed description.



## Serial Interface Description

I<sup>2</sup>C is a 2 wire serial interface. The bus consists of a data line (SDA) and a clock line (SCL) with a pull-up device. When the bus is idle, both SDA and SCL lines are pulled high. All I<sup>2</sup>C compatible devices connect to the I<sup>2</sup>C SDA and SCL buses through open drain I/O pins. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific condition that indicates the START and STOP of data transfer. A slave device receives and /or transmits data on the bus under control of the master device.

HL7007 works as a slave and is compatible with the following data transfer modes as defined in the I<sup>2</sup>C Bus Specification: Standard mode (100kbps), Fast mode (400kbps), Fast mode plus (1000kbps) and High-speed mode (up to 3.4Mbps in write mode). The interface adds flexibility to the battery charge solution by making most functions and parameters programmable through the I<sup>2</sup>C host.

The data transfer protocol for Standard mode, Fast mode and Fast mode plus is the same, therefore referred to as F/S mode in this document. The protocol for High-speed mode is different and referred to as HS-mode.

### F/S Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high. The master stops data transfer by generating a STOP condition, in which a low-to-high transition occurs on the SDA line while SCL is high. This is shown in Figure 19.

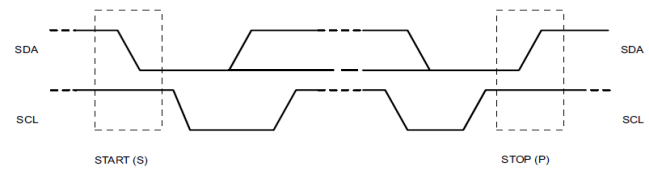


Figure19. START and STOP Condition

After START condition, the master generates SCL pulse, and transmits 7-bit slave address and the read/write bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 20.)

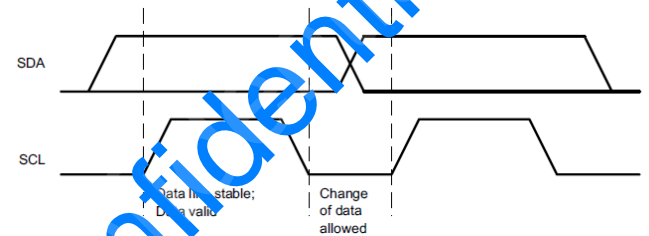


Figure 20. Bit Transfer on the Serial Interface

All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 21) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge signal, the master knows that communication link with a slave has been established.

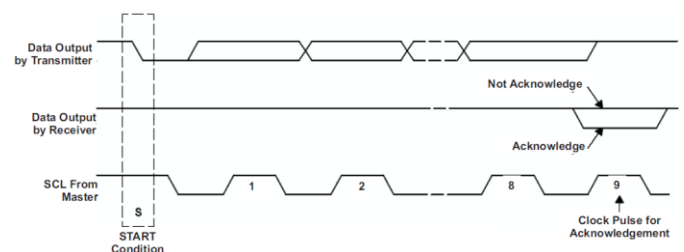


Figure 21. Acknowledge on the I<sup>2</sup>C Bus

The master generates further SCL cycles to either transmit data to the slave (R/W bit =1) or receive data

from the slave (R/W bit =0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a STOP condition (see Figure 22). This releases the bus and stops the communication link with the addressed slave.

All I<sup>2</sup>C compatible devices must recognize the STOP condition. Upon receiving the STOP condition, all devices know that the bus is released, and they wait for a start byte followed by a matching address. If a transmission is terminated prematurely, the master needs to send a STOP condition to prevent the slave I<sup>2</sup>C logic from getting stuck in a bad state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

1Mbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4Mbps operation.

The master then generates a Repeated Start condition (a Repeated START condition has the same timing as the start condition). After this Repeated START condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A STOP condition ends the H/S mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a STOP condition, repeated start conditions should be used to secure the bus in HS mode. If a transmission is terminated in advance, the master needs sending a STOP condition to prevent the slave I<sup>2</sup>C logic from getting stuck in a bad state.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

## I<sup>2</sup>C Update Sequence

The IC requires a START condition, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single update. After receiving of each byte, the IC sends acknowledge by pulling the SDA line low during the high period of a single clock. A valid I<sup>2</sup>C address will select this IC. The IC performs an update on the falling edge of the acknowledge signal that follows the LSB bit.

For the first update, the IC requires a START condition, a valid I<sup>2</sup>C address, a register address byte and a data byte. For all consecutive updates, the IC needs a register address byte and a data byte. Once a STOP condition is received, the IC releases the I<sup>2</sup>C bus and waits for a new START condition.

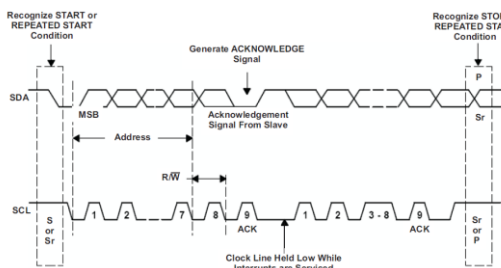
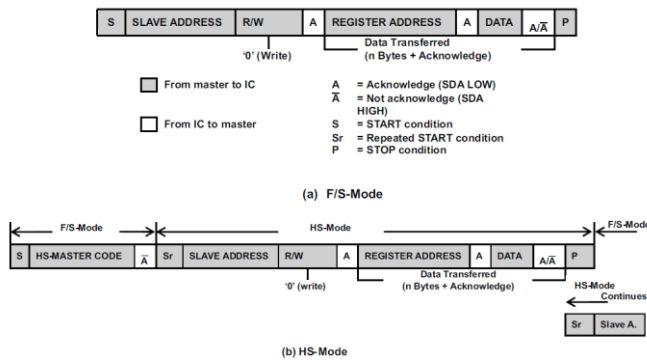


Figure 22. Bus Protocol

## H/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a START byte followed by a valid serial byte containing HS master code 0000 1XXX. This transmission is made in F/S-mode with speed less than



## Slave Address Byte

MSB

LSB

1	1	0	1	0	1	0	X
---	---	---	---	---	---	---	---

The slave address byte is the first byte received following the START condition from the master device.

## Register Description

Register		Address Bits							
Name	Hex Address	7	6	5	4	3	2	1	0
CHG_STATUS	00H	0	0	0	0	0	0	0	0
CHG_CONTROL0	01H	0	0	0	0	0	0	0	1
OREG	02H	0	0	0	0	0	0	1	0
IC_INFO	03H	0	0	0	0	0	0	1	1
IBAT	04H	0	0	0	0	0	1	0	0
CHG_CONTROL1	05H	0	0	0	0	0	1	0	1
SAFETY	06H	0	0	0	0	0	1	1	0
MONITOR0	10H	0	0	0	1	0	0	0	0

Table 4. Register map of HL7007

## Bit Definitions

The following table defines the operation of each register bit. Bold font indicates power-on default values.

Bit	Name	Value	Type	Function	
CHG_STATUS		Register Address: 00		Default Value:X1XX 0XXX	
7	TMR_RST/ OTG	1	W	Write 1 reset safety timer (automatic clearance); write “0” has no effect	
			R	Return the OTG pin status (1 =high)	
6	EN_STAT	0	R/W	Disable the STAT pin function	
		1		Enable the STAT pin function	
5:4	STAT	00	R	Ready	
		01		Allow PWM charging. If CE=0, charging.	
		10		Charge termination	
		11		Fault (fault status)	
3	BOOST	0	R	IC is not in BOOST mode	
		1		IC is in BOOST mode	
2:0	FAULT		R	Charge mode	Boost mode
		000		Normal(No Fault)	Normal(No Fault)
		001		VIN OVP	VIN OVP
		010		Sleep Mode	Boost soft start failure
		011		Poor Input Source	V <sub>BAT</sub> <UVLOBST
		100		Output OVP	Battery OVP
		101		Thermal Shutdown	Thermal Shutdown
		110		Timer Fault	Timer Fault; reset all registers
		111		No Battery	N/A
		CHG_CONTROL0		Register Address: 01	
7:6	I <sub>INLIM</sub>	00	R/W	100mA	USB host limit for input current
		01		500mA	
		10		800mA	
		11		No limit for input current	
5:4	V <sub>LowV</sub>	00	R/W	3.4V	Weak battery threshold
		01		3.5V	
		10		3.6V	
		11		3.7V	
3	TE	0	R/W	Disable charge termination function	
		1		Enable charge termination function	
2	CE	0	R/W	Enable charge function	
		1		Disable charge function	
1	HZ_MODE	0	R/W	Disable High-Z mode	

		1		Enable High-Z mode									
0	OPA_MODE	0		Charge mode									
		1		Boost mode									
OREG		Register Address: 02		Default Value:1000 1110									
7:2	OREG		R/W	Charge termination voltage, programmable every step 20mV. Default value 100011 (4.2V)									
				HEX	V <sub>OREG</sub>	HEX	V <sub>OREG</sub>	HEX	V <sub>OREG</sub>				
				00	3.50	10	3.82	20	4.14				
				01	3.52	11	3.84	21	4.16				
				02	3.54	12	3.86	22	4.18				
				03	3.56	13	3.88	23	4.20				
				04	3.58	14	3.90	24	4.22				
				05	3.60	15	3.92	25	4.24				
				06	3.62	16	3.94	26	4.26				
				07	3.64	17	3.96	27	4.28				
				08	3.66	18	3.98	28	4.30				
				09	3.68	19	4.00	29	4.32				
				0A	3.70	1A	4.02	2A	4.34				
				0B	3.72	1B	4.04	2B	4.36				
				0C	3.74	1C	4.06	2C	4.38				
				0D	3.76	1D	4.08	2D	4.40				
				0E	3.78	1E	4.10	2E	4.42				
				0F	3.80	1F	4.12	2F~3F	4.44				
				1	OTG_PL	0	R/W	OTG pin Low valid					
						1		OTG pin High valid					
0	OTG_EN	0	R/W	In host mode, disable OTG pin									
		1		In host mode, Enable OTG pin									
IC_INFO		Register Address: 03		Default Value:010X XXXX									
7:5	Vendor Code	010	R	This IC vendor number									
4:3	PN		R	Part Number									
2:0	REV		R	IC version									
IBAT		Register Address: 04		Default Value:0000 0001									
7	RESET	0	R/W	Writing 0 has no effect.(Note: read always returns 1)									
		1		Reset all registers except Safety register (Reg6)									
				Note: Rsns=68 mΩ									
6:4	IOCHARGE	0000	R/W	550mA									

		0001		650mA	
		0010		750mA	
		0011		850mA	
		0100		1050mA	
		0101		1150mA	
		0110		1350mA	
		0111		1450mA	
		1000		1550mA	
		1001		1650mA	
		1010		1750mA	
		1011		1850mA	
		1100		2050mA	
		1101		2150mA	
		1110		2350mA	
		1111		2450mA	
3	Reserved	0	R/W	N/A	
2:0	I <sub>TERM</sub>	000	R/W	50mA	Charge termination current
		001		100mA	
		010		150mA	
		011		200mA	
		100		250mA	
		101		300mA	
		110		350mA	
		111		400mA	
CHG_CONTROL1			Register Address: 05	Default Value:001X X100	
7:6	NA		R/W	NA	
5	IO_LEVEL	0	R/W	Charge current controlled by register IOCHARGE	
		1		Charge current fixed at 500mA	
4	SP	0	R	VIN loop not in control (VIN still above voltage limit threshold)	
		1		VIN loop in control (VIN within limit threshold)	
3	EN_LEVEL	1	R	CDIS is high	
		0		CDIS is low	
2:0	VSP	000	R/W	4.213V	VIN loop control threshold
		001		4.293V	
		010		4.373V	
		011		4.453V	

		100		4.533V	
		101		4.613V	
		110		4.693V	
		111		4.773V	
SAFETY Register Address: 06 Default Value:0100 0000					
7	Reserved	0	R		
6:4	ISAFE	000	R/W	550mA	Set the maximum Charge current IOCHARGE. Default value 0100 (1050mA) .  The I <sup>2</sup> C master has to write this register in its first communication after IC power up, otherwise default value will be locked until chip POR or V <sub>BAT</sub> falls below V <sub>SHORT</sub> .
		001		650mA	
		010		750mA	
		011		850mA	
		100		1050mA	
		101		1150mA	
		110		1350mA	
		111		1450mA	
3:0	VSAFE	0000		4.20V	Set the maximum battery voltage.  The I <sup>2</sup> C master has to write this register in its first communication after IC power up, otherwise default value will be locked until chip POR or V <sub>BAT</sub> falls below V <sub>SHORT</sub> .
		0001		4.22V	
		0010		4.24V	
		0011		4.26V	
		0100		4.28V	
		0101		4.30V	
		0110		4.32V	
		0111		4.34V	
		1000		4.36V	
		1001		4.38V	
		1010		4.40V	
		1011		4.42V	
		1100		4.44V	
		1111			
MONITOR Register Address: 10 Default Value: XXXX XXXX					
7	ITERM_CMP		R	ITERM comparator output. 1 means ICHARGE>ITERM	
6	VBAT_CMP		R	V <sub>BAT</sub> comparator output. 1 means V <sub>USB</sub> >V <sub>ICSN</sub>	
5	LINCHG		R	30mA linear charge status. 1 means linear charge running.	
4	T_120		R	120C Over temperature protection. When T_120=1 and T_145=0, charge current will be limited.	
3	ICHG		R	0 indicates ICHARGE loop is controlling charge current.	
2	IVUSB		R	0 indicates IUSB loop (input current) is controlling charge current.	

1	VUSB_VALID		R	1 indicates VUSB can be use to charge after detection.
0	CV		R	1 indicates Constant Voltage loop is in control of charging.

Table 5. Register map of HL7007. Bold characters indicate default values upon POR.

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## Application Information

### Interrupt (STAT Pin) Description

STAT is an open-drain output pin. It drives a pull-up resistor and informs the host of HL7007 working status. In normal conditions its output is high. In fault conditions, a 128-μs pulse is sent to notify the host.

Status	STAT Pin
Charge & EN_INT=1	LOW
Other normal conditions	OPEN
Charge mode fault: Timer fault, Sleep Mode, $V_{USB}/V_{BAT}$ OVP, $V_{USB}$ UVLO, Poor input source, Battery absent, Thermal shutdown	128-μs pulse, then OPEN
Boost mode fault: Timer fault, Over load, $V_{USB}/V_{BAT}$ OVP, $V_{BAT}$ UVLO, Thermal shutdown	128-μs pulse, then OPEN

Table 6. STAT Signal

### Over Temperature Limit and Protection

In the charging process, in order to prevent the IC from overheating, HL7007 will monitor its junction temperature  $T_J$  to prevent the IC from overheating. Once the temperature reaches the thermal limit threshold  $T_{CF}$ , the IC will reduce the charging current. If  $T_J$  has reached  $T_{SHTDWN}$ , the IC will suspend charging. Under this thermal-protection mode, the PWM controller will shut down and all timers freeze. When  $T_J$  drops below  $T_{SHTDWN}$  by about 20°C, the IC resumes charging.

### USB Plug-In

Before the USB power is plugged in, the I<sup>2</sup>C host can keep writing 1 to TMR\_RST so the chip stays in host mode. Once USB power is plugged in, HL7007 will enter normal charge mode using parameters from the register set. If the

IC is not in host mode when USB power is plugged in, IC will work in 30-minute mode, in which the IC will charging for 30 minutes with default charging parameters, until the host communicates with the IC.

The default values of the registers are set at low level of charging current and termination voltage. This prevents violation of USB specification or over-charging any type of lithium-ion batteries. At the same time the termination voltage is set high enough to prevent the I<sup>2</sup>C host from losing power supply.

### Charge Current Sensing Resistor Selection Guidelines

Both the termination current and charge current depend on the external sensing resistor ( $R_{SNS}$ ). The termination current step ( $I_{TERM\_STEP}$ ) can be calculated using Equation 1:

$$I_{(TERM\_STEP)} = \frac{V_{I(TERM0)}}{R_{(SNS)}}$$

Table 7 shows the setup of termination current for three sensing resistors.

For example, with a 68mΩ sense resistor,

$V_{I(TERM2)}=1, V_{I(TERM1)}=0$ , and  $V_{I(TERM0)}=1$ , then  $I_{TERM} = [ (13.6mV \times 1) + (6.8mV \times 0) + (3.4mV \times 1) + 3.4mV ] / 68m\Omega = 200mA + 0 + 50mA + 50mA = 300mA$ .

BIT	$V_{I(TERM)}$ (mV)	$I_{(TERM)}$ (mA) $R_{(SNS)} =$ 56mΩ	$I_{(TERM)}$ (mA) $R_{(SNS)} =$ 68mΩ	$I_{(TERM)}$ (mA) $R_{(SNS)} =$ 100mΩ
$V_{I(TERM2)}$	13.6	242	200	136
$V_{I(TERM1)}$	6.8	124	100	68
$V_{I(TERM0)}$	3.4	61	50	34
Offset	3.4	61	50	34

Table 7. Termination Current Setting

$$I_{O(CHARGE\_STEP)} = \frac{V_{I(CHRG0)}}{R_{(SNS)}}$$

BIT	V <sub>I(REG)</sub> (mV)	I <sub>O(CHARGE)</sub> (mA) R <sub>(SNS)</sub> = 56mΩ	I <sub>O(CHARGE)</sub> (mA) R <sub>(SNS)</sub> = 68mΩ	I <sub>O(CHARGE)</sub> (mA) R <sub>(SNS)</sub> = 100mΩ
V <sub>I(CHRG3)</sub>	54.4	971	800	544
V <sub>I(CHRG2)</sub>	27.2	486	400	272
V <sub>I(CHRG1)</sub>	13.6	242	200	136
V <sub>I(CHRG0)</sub>	6.8	122	100	68
Offset	37.4	668	550	374

Table 8. Charge Current Setting

For example, with a 68-mΩ sense resistor, V(CHRG3) = 1, V(CHRG2) = 0, V(CHRG1) = 0, and V(CHRG0) = 1,  $I_{TERM} = [(54.4 \text{ mV} \times 1) + (27.2 \text{ mV} \times 0) + (13.6 \text{ mV} \times 0) + (6.8 \text{ mV} \times 1) + 37.4 \text{ mV}] / 68 \text{ m}\Omega = 800 \text{ mA} + 0 + 0 + 100 \text{ mA} = 900 \text{ mA}$ .

## PCB Layout Reference

PCB layout is important to optimal HL7007 performance. The following provides some guidelines:

(1) To obtain optimal performance, the power input capacitors, connected from power input to PGND, should be placed as close to the IC as possible. The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intention is to minimize the current path loop area (from the SW pin through the LC filter to the PGND pin and back to IC). To prevent high frequency oscillation problem, use proper layout to minimize high frequency current path loop (See Figure 24). The sense resistor should be close to the junction of the output capacitor and inductor. The sense path must connect to the underneath

## Output Inductor and Capacitance Selection Guidelines

HL7007 provides full internal loop compensation. With the internal loop compensation, the highest stability occurs when the LC resonant frequency  $f_o$ , is approximately 40 kHz (20 kHz to 80 kHz). Equation 3 can be used to calculate the value of the output inductor  $L_{OUT}$ , and output capacitor  $C_{OUT}$ .

$$f_o = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 22 μF and 100 μF is recommended for  $C_{OUT}$ .

of the resistor, and do not cross any high-current path.

(2) Place all decoupling capacitors close to their respective IC pins and close to PGND. Do not place components on any high-current path. All small control signals should be kept away from any high current path.

(3) The PCB should have a dedicated ground plane, which is connected to all components through via holes (two via holes per power-stage capacitors; two via holes for the IC PGND; one via per capacitor of small-signal components). Use star connection to separate different parts (high-power/low-power/small-signal) of the application design to reduce coupling noise and ground noise. Using small-size layout and independent ground connection will

reduce ground noise and minimize coupling between signals.

(4) The high-current charge paths of VBUS, PMID, SW and PGND pins must be sized appropriately according to their maximum charge current in order to minimize voltage drops on their PCB routes. The PGND trace carry the return current from the internal low-side power FET, and should also be connected to the ground plane.

(5) Place the 4.7 $\mu$ F input capacitor as close to VPRT and PGND pins as possible to minimize high frequency input current loop area . Place the VUSB capacitor as close to VBUS and PGND pins as possible for the same reason.

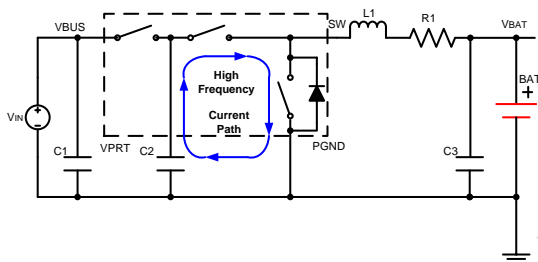


Figure 24. High Frequency Current Path

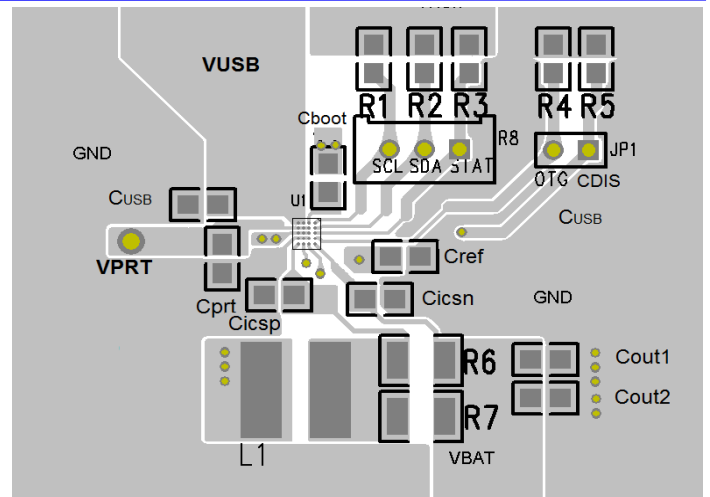


Figure 25. Top Layer

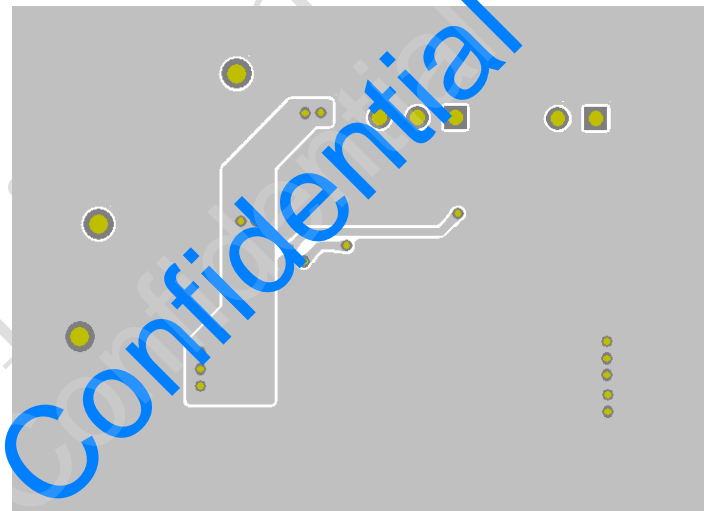
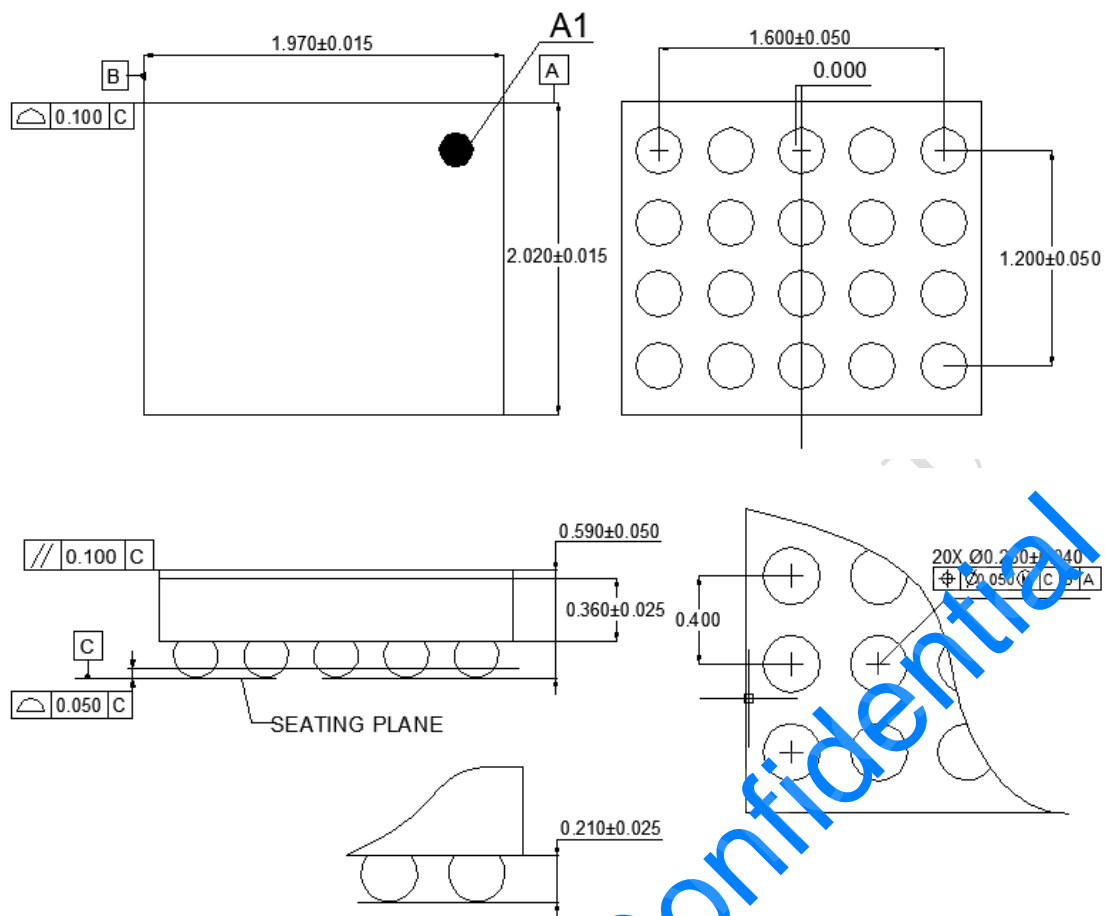


Figure 26. Bottom Layer

## Package Information

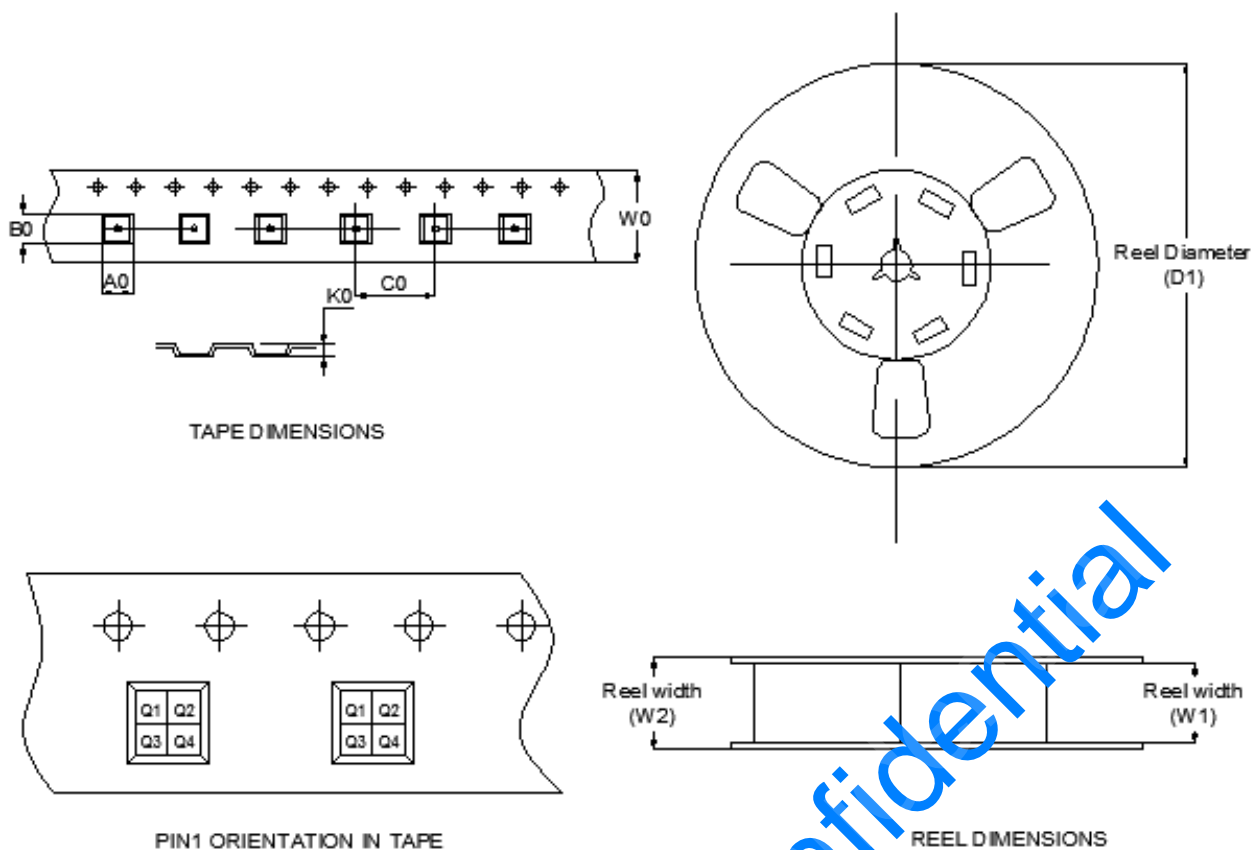


WLCSP20-Ball, 4X5Array, 0.4mm Pitch, 1.970mmx2.020mm package

### NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

## Tape and Reel Information



Device	Package	SPQ	D1	W1	W2	A0	B0	K0	C0	W0	PIN1
HL7007	WLCSP- 20	3000	180 +0/-1	9.00 (min)	2.4 (max)	2.13 ±0.05	2.13 ±0.05	0.88 ±0.05	4.00 ±0.1	8.00 +0.3/-0.1	Q1

### NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS ARE NOMINAL.

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